Specification Amendments

Please replace the previous BACKGROUND OF THE INVENTION with the amended one provided below.

BACKGROUND OF THE INVENTION

Field of the Invention

This invention is directed to an analysis of a waveform for a telecommunication system or for a measurement equipment, and more particularly to a Digital Signal Processing of Multi-Sampled Phase (DSP MSP).

The DSP MSP allows waveform analysis, noise filtering, and data recovery for wireless, optical , or wireline transmission systems and measurement systems and for a wide range of data rates and waveform timings.

The invention further includes Sequential Data Recovery from Multi Sampled Phase (SDR MSP), which is a version of the DSP MSP, which provides clock and data recovery for optical communications.

Background Art

Background art for this invention is represented by the documents listed below:

D1 (US 5,668,830 by Georgiu Christos John ET AL)

D2 (PCT/CA01/00723 invented by Bogdan);

D3 (US 2002/0009171 invented by Ribo);

D4 (US 5,592,125 invented by Williams);

<u>D5 (US 6,987,817 invented by Reuveni)</u>

The D1 is limited to using delay lines and most basic digital filters for removing phase noise of waveform edges. D1 circuits enable merely edge phase aligning and data re-timing on a bit per bit basis for data serializing/de-serializing only.

Consequently, D1 circuits do not have any of the fundamental features of the present

invention such as; over-sampling and noise filtering from entire pulse necessary for elimination of noise occurring inside data pulses, or cumulative processing operations necessary for measuring and processing lengths of transmitted pulses, or adaptive signal processing using wave-form screening.

The D2 solution created variety of high resolution phase capturing techniques which are useful for measuring phase skews between low frequency frames in high quality synchronization circuits. However these D2 phase capturing techniques have never been targeting any processing throughput which could be even close to that needed for communication signal processing. Therefore besides said high resolution phase capture, the D2 solution has fundamentally different principle of operation and produces entirely different results.
Consequently D2 can not contribute to any processing of much higher frequency signals commonly used in communication links.

The D3 solution represents latest generation of clock and data recovery (CDR) circuits which over-sample in expected transition region in order to achieve some fractional improvements of jitter tolerance.
The D3 captures windows consisting of samples covering entire data bit interval.
Every such window covers single bit interval only and it is captured and processed separately from other windows on a bit interval by bit interval basis without any correlation between data captured in consecutive windows. Such lack of correlation amounts to inability to filter out narrow glitches occurring between windows.
Therefore the D3 windows need to be centered around expected edges of received data bits in order to enable said bit by bit processing without data recovery errors.
Obviously such window centering can only be achieved by phase locking to the received signal.

Other over-sampling solution is the CDR with bang-bang phase detector (CDR with BBPD) represented by D4.
While taking more samples provides D3 with better base for jitter filtering than that of the CDR with BBPD, dynamics of D3 phase locking has to accommodate additional interference caused

by said jiter filtering and by further processing of output data providing return reference for the D3 phase locked loop.

Similarly as the D3 and the CDR with BBPD, all other conventional analyzers and receivers of serial data have the same common feature limiting severely their performances; they require phase locking to received signal in order to recover data based on sampling localized in a credible region of the received wave-form.

The phase locking requirement is not only difficult to achieve but furthermore it imposes significant limitations on receiver performances such as those listed below:

- Jitter tolerance is very low outside the bandwidth of receivers PLL while such PLLs bandwidth is usually below 1/10 of the bandwidth of transmitted signals which are the major sources of phase jitter and amplitude noise.
- Such receivers are defenseless against high frequency noise occurring in wave-form regions which can not be filtered out using said localized sampling.
- Such PLL based receivers require significant lock acquisition times before newly established data link becomes operational what is an impediment for all burst types of data links.

Still other over-sampling solution is described in D5 as designed originally for processing serial data streams from a recordable medium like CD or DVD. Nevertheless some of D5 teachings describe data recovery circuits, which derive number of data bits received in a waveform pulse by dividing a length of the pulse by a bit widths calculated statistically by processing received signal wavefroms. Such pulse lengths is calculated originally as a sum of all oversampling sub-clocks occurring during the pulse, and is divided by such statistically calculated bit width later on.

However such calculations of the sub-clocks sum and such divisions involving long pulses, limit data rates which D5 solution can be utilized at. Furthermore limited accuracy of such statistically calculated bit widths and division error accumulated during any long pulse processing, increase error rates and limit reliability. Still furthermore; since such statistical processing of the bit widths is performed in a closed loop, it can cause stability problems due to highly unpredictable phase noise in the received signal.

This invention is based on fundamentally different principle of operation relying on; measurements of pulse lengths of incoming wave-form with accuracy matching single gate delays, and on digital processing of such accurate pulse lengths in order to recover data transmitted by the wave-form or to analyze the waveform.

Such superior principle of operation combined with adaptive signal processing algorithms utilizing verification of received waveforms, eliminate all the above deficiencies of the conventional solutions and enable significantly longer transmission distances.

3. Citations List

1. US 5,668,830 Georgiu, 16 September 1997
2. PCT/CA01/00723 / W0 01 91297 Bogdan, 29 November 2001
3. US 2002/0009171 Ribo, 24 January 2002
4. US 5,592,125 Williams, 7 January 1997
5. US 6,987,817 Reuveni, 17 January 2006
6. US 4,977,582 Zelle, 11 December 1990
7. US 5,467,464 Oprescu, 14 November 1995
8. US 5,872,791 Propp, 16 February 1999
9. EP 0 292 208 American Telephone & Telegraph, 23 November 1988

Please insert BRIEF DESCRIPTION OF THE DRAWINGS provided below after SUMMARY OF THE INVENTION and before DESCRIPTION OF THE PREFERRED EMBODIMENTS.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG.1A shows Block Diagram of Sequential Data Recovery in order to introduce major sub-systems and interfaces shown in the next drawings numbered as FIG.1 - FIG.4B.

Such next drawings are numbered correspondingly to processed data flow.
All interconnect signals between the next drawings have unique names identifying their sources and destinations explained in the Description of the Preferred Embodiments utilizing the same names.
Inputs supplied from different drawings are connected at the top or left side and outputs are generated on the bottom due to the top-down or left-right data flow observed generally.
Clocked circuits like registers or flip-flops are drawn with two times thicker lines than combinatorial circuits like arithmometers or selectors.

FIG.1 shows Sampling Clocks and Wave Capturing circuits generating sub-clocks of a sampling clock and utilizing them to capture samples of incoming waveform.

FIG.2A shows Sequential Clocks Generation (SCG) circuits providing sequential clocks suitable for synchronizing processing stages working in multistage and/or multiphase configurations.

FIG.2B shows Sequential Phase Control (SPC) circuits utilizing such sequential clocks and signals from the processing stages for assigning different processing phases for processing consecutive inter-transition intervals and for controlling operations of such processing stages.

FIG.2C shows Timing Diagram of the Sampling Clock and Waveform Capturing.

FIG.2D shows Timing Diagram of the Sequential Phase Control being continuation of FIG.2C proceeded by a phase2 long data string.

FIG.3A shows Phase1 of the Phase Processing Stages controlled by Mask Registers and Control Registers programmed by PCU.

FIG.3B shows Periodical Skew Accumulation circuits enabling elimination of phase skew errors, between the sampling clock and received data bits, accumulated over received data string.

FIG.3C shows Received Data Collection circuits.

FIG.3D shows Data Frequency Capturing circuits for measuring frequency difference between data bits and sampling clock.

FIG.4A shows Wave Form Screening & Capturing (WFSC) circuit enabling screening and capturing incoming waveform within time intervals programmed by PCU.

FIG.4B shows Timing Diagrams of the WFSC.